IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A hybrid built-in self test (BIST) architecture for embedded memory arrays that segments BIST functionality into remote lower-speed executable instructions and local higher-speed executable instructions, the architecture comprising:

a ~~standalone~~ BIST logic controller that is separate from said embedded memory arrays, is adapted to ~~operating~~ operate at a lower frequency than said embedded memory arrays, and is further adapted to perform test functions common to all of said embedded memory arrays at said lower frequency ~~and being adapted to communicate with a plurality of embedded memory arrays using a BIST instruction set~~; and

a plurality of blocks of ~~higher speed~~ test logic in communication with said BIST logic controller,

wherein each one of said blocks is incorporated into ~~each~~ a corresponding one of said embedded memory arrays under test, is adapted to operate at a same frequency as said corresponding one of said embedded memory arrays, and is further adapted to perform test functions unique to said corresponding one of said embedded memory arrays at said same frequency,

wherein said same frequency comprises a higher frequency relative to said lower frequency of said BIST logic controller,

wherein said BIST logic controller is further adapted to communicate, to each of said blocks, instructions at said lower frequency, and

wherein said each of said blocks is further ~~being~~ adapted to locally process said ~~BIST~~ instructions at said higher frequency ~~received from said standalone BIST logic controller at a higher frequency than said lower frequency~~.

2. (Currently Amended) The hybrid BIST architecture in claim 1, wherein said ~~higher-speed test logic includes~~ blocks of test logic each comprise a multiplier for increasing the frequency of said ~~BIST~~ instructions from said lower frequency to said higher frequency.

3. (Currently Amended) The hybrid BIST architecture in claim 1, wherein each of said blocks of test logic comprises: ~~said standalone BIST logic controller enables a plurality of higher-speed test logic structures in a plurality of embedded memory arrays~~

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic adapted to decode each of said instructions received from said BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays,

wherein said data address control generation logic and said redundancy allocation logic are adapted to use said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

4. (Currently Amended) The hybrid BIST architecture in claim 1, wherein said ~~standalone~~ BIST logic controller in combination with said blocks enables in parallel testing of at least one of the following:

different types of embedded memories, wherein said different types comprise at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

5. (Currently Amended) The hybrid BIST architecture in claim 1, further comprising a lower-speed control bus operating at said lower frequency and connecting said ~~standalone~~ BIST logic controller to said blocks ~~higher-speed test logic~~ so as to allow communication of said instructions from said BIST logic controller to said blocks.

6. (Currently Amended) The hybrid BIST architecture in claim 1, wherein said ~~standalone~~ BIST logic controller comprises at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets.

7. (Currently Amended) The hybrid BIST architecture in claim 1, wherein said ~~standalone~~ BIST logic controller comprises logic adapted to provide branch prediction, program counter management, utility counters, and general BIST operation controls and

diagnostic outputs.

8. (Currently Amended) A built-in self test (BIST) architecture for use with embedded memory arrays ~~embedded~~ in functional circuitry within an integrated circuit, said BIST architecture comprising:

a BIST logic controller that is separate from said embedded memory arrays, is adapted to operate at a lower frequency than said embedded memory arrays, and is further adapted to perform test functions common to all of said embedded memory arrays at said lower frequency;

a plurality of ~~embedded~~ blocks of test logic ~~incorporated into embedded memory arrays;~~

~~a remote BIST logic controller, separate from said embedded blocks of test logic;~~ and

a bus connecting said ~~remote~~ BIST logic controller to each of said ~~embedded~~ blocks of test logic so as to allow communication from said BIST logic controller to said blocks,

wherein said bus is adapted to operate at said lower frequency,

wherein each one of said blocks is incorporated into a corresponding one of said embedded memory arrays, is adapted to operate at a same frequency as said corresponding one of said embedded memory arrays, and is further adapted to perform test functions unique to said corresponding one of said embedded memory arrays,

wherein said same frequency comprises a higher frequency relative to said lower

frequency of said BIST logic controller and said bus,

wherein said ~~remote~~ BIST logic controller is further adapted to communicate, to each of said blocks, instructions at said lower frequency via said bus ~~performs functions that are common to all of said embedded blocks of test logic~~, and

wherein said each of said blocks is further adapted to locally process said instructions at said higher frequency ~~remote BIST logic controller and said bus operate at a lower frequency than said embedded blocks of test logic~~.

9. (Currently Amended) The BIST architecture in claim 8, wherein said ~~embedded~~ blocks of test logic each ~~include~~ comprise a multiplier for increasing the frequency of ~~BIST~~ said instructions from said lower frequency to said higher frequency ~~received from said BIST logic controller to a higher frequency of a corresponding embedded memory array~~.

10. (Currently Amended) The BIST architecture in claim [[8]] 11, wherein ~~each of said embedded blocks of test logic includes unique logic blocks that are unique to a corresponding embedded memory array~~ said data address control generation logic and said redundancy allocation logic are adapted to use said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

11. (Currently Amended) The BIST architecture in claim 8, wherein each of said ~~embedded~~ blocks of test logic ~~includes~~ comprises:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic adapted to decode each ~~macro instruction sets~~ of said instructions received from said ~~remote~~ BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

12. (Currently Amended) The BIST architecture in claim 8, wherein said ~~remote~~ BIST logic controller in combination with said blocks enables in parallel testing of at least one of the following :

different types of embedded memories, wherein said different types comprise at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

13. (Currently Amended) The BIST architecture in claim 8, wherein said ~~standalone~~ BIST logic controller comprises at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets.

14. (Currently Amended) The BIST architecture in claim 8, wherein said ~~remote~~ BIST logic controller comprises logic adapted to provide branch prediction, program counter management, utility counters, and general BIST operation controls and diagnostic outputs.

15. (Currently Amended) A built-in self test (BIST) architecture for use with embedded memory arrays ~~embedded~~ in functional circuitry within an integrated circuit, said BIST architecture comprising:

a BIST logic controller that is separate from said embedded memory arrays, is adapted to operate at a lower frequency than said embedded memory arrays, and is further adapted to perform test functions common to all of said embedded memory arrays at said lower frequency;

a plurality of ~~embedded~~ blocks of test logic ~~incorporated into embedded memory arrays~~;

~~a remote BIST logic controller, separate from said embedded blocks of test logic;~~ and

a bus connecting said ~~remote~~ BIST logic controller to said each of said ~~embedded~~ blocks of test logic so as to allow communication from said BIST logic controller to said blocks,

wherein said bus is adapted to operate at said lower frequency,

wherein each one of said blocks is incorporated into a corresponding one of said

embedded memory arrays, is adapted to operate at a same frequency as said corresponding one of said embedded memory arrays, and is further adapted to perform test functions unique to said corresponding one of said embedded memory arrays,

wherein said same frequency is a higher frequency relative to said lower frequency of said BIST logic controller and said bus,

~~wherein said remote BIST logic controller and said bus operate at a lower frequency than said embedded blocks of test logic, and~~

wherein said ~~remote~~ BIST logic controller is further adapted to communicate, to each of said blocks, instructions at said lower frequency via said bus ~~performs functions that are common to all of said embedded~~,

wherein said each of said blocks is further adapted to locally process said instructions at said higher frequency, and

wherein said test functions that are common to all of said embedded memory arrays comprise ~~blocks of test logic including~~ providing branch prediction, program counter management, utility counting, and general BIST operation control and diagnostic outputs.

16. (Currently Amended) The BIST architecture in claim 15, wherein said ~~embedded~~ blocks of test logic each ~~include~~ comprise a multiplier for increasing the frequency of ~~BIST~~ said instructions from said lower frequency to said higher frequency ~~received from said BIST logic controller to a higher frequency of a corresponding embedded memory array~~.

17. (Currently Amended) The BIST architecture in claim [[15]] 18, wherein ~~each of said embedded blocks of test logic includes unique logic blocks that are unique to a corresponding embedded memory array~~ said data address control generation logic and said redundancy allocation logic are adapted to use said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

18. (Currently Amended) The BIST architecture in claim 15, wherein each of said ~~embedded~~ blocks of test logic comprises ~~includes~~:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic adapted to decode each of said instructions ~~macro-instruction sets~~ received from said ~~remote~~ BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

19. (Currently Amended) The BIST architecture in claim 15, wherein said ~~remote~~ BIST logic controller in combination with said blocks enables in parallel testing of at least one of the following:

different types of embedded memories, wherein said different types comprise at least one of a dynamic random access memory (DRAM) array, a static random access

memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

20. (Currently Amended) The BIST architecture in claim 15, wherein said ~~standalone~~ BIST logic controller comprises at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets.

21. (Cancelled).

22. (Currently Amended) A method of testing embedded memory arrays ~~embedded~~ in functional circuitry within an integrated circuit using a built-in self test (BIST) architecture, said method comprising:

performing, by a BIST logic controller, ~~BIST~~ test functions ~~that are~~ common to all of said embedded ~~blocks of test logic incorporated into each embedded~~ memory arrays,

wherein said BIST logic controller is remote from said embedded memory arrays and operates at a lower frequency than said embedded memory arrays ~~using a separate BIST logic controller, separate from said embedded blocks of test logic~~;

sending, by said BIST logic controller, ~~BIST~~ instructions ~~from said remote BIST logic controller~~ to ~~said embedded~~ a plurality of blocks of test logic,

wherein each one of said blocks is incorporated into a corresponding one of said embedded memory arrays and operates at a same frequency as said corresponding one of said embedded memory array, and

wherein said same frequency comprises a higher frequency relative to said lower frequency of said BIST logic controller; and

performing, by each of said blocks, test functions unique to said corresponding one of said embedded memory arrays, wherein said performing comprises:

increasing the frequency of ~~BIST~~ said instructions ~~received from said BIST logic controller, using said embedded blocks of test logic, to a~~ to said higher frequency ~~of a corresponding embedded memory array~~.

23. (Currently Amended) The method in claim 22, wherein said sending ~~of BIST instructions from said remote BIST logic controller to said embedded blocks of test logic uses~~ comprises using a bus connecting said ~~remote~~ BIST logic controller to said ~~embedded~~ blocks of test logic so as to allow communication of said instructions from said BIST logic controller to said blocks, wherein said bus operates at ~~the same~~ said lower frequency [[as]] of said ~~remote~~ BIST logic controller.

24. (Currently Amended) The method in claim [[22]] 25, ~~further comprising performing unique testing via logic blocks that are unique to a corresponding embedded memory array at each of said embedded blocks of test logic~~ wherein said performing of data address control generation and said performing of said redundancy allocation are

based on said individual micro-instructions.

25. (Currently Amended) The method in claim 22, wherein said performing, by each of said blocks, comprises: ~~each of said embedded blocks of test logic performs the following processes~~:

~~multiplying BIST instructions received from said remote BIST logic controller;~~

performing redundancy allocation;

performing data address control ~~and~~ generation; and

decoding each of said instructions ~~macro instruction sets~~ received from said ~~remote~~ BIST logic controller into individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

26. (Currently Amended) The method in claim 22, wherein said performing by said BIST logic controller of said test functions common to all of said embedded memory arrays and said performing by said each of said blocks of said test functions unique to said corresponding one of said embedded memory arrays ~~said sending process performed by said remote BIST logic controller~~ enables in parallel testing of at least one of the following:

different types of embedded memories, wherein said different types comprise at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

27. (Currently Amended) The method in claim 22, further comprising storing said instructions ~~macro instruction sets~~ in one of read only memories (ROMs), a scannable read only memory (SROM), and other type of memory in said ~~remote~~ BIST logic controller.

28. (Currently Amended) The method in claim 22, wherein said performing by said BIST logic controller of said test functions common to all of said embedded memory arrays comprises performing: ~~further comprising providing, by said remote BIST logic controller~~:

branch prediction;

program counter management;

utility counting; and

general BIST operation control and diagnostic outputs.

29. (Currently Amended) A method of testing embedded memory arrays ~~embedded~~ in functional circuitry within an integrated circuit using a built-in self test (BIST) architecture, said method comprising:

performing, by a BIST logic controller, ~~BIST~~ test functions ~~that are~~ common to all of said ~~embedded blocks of test logic incorporated into each~~ embedded memory arrays,

wherein said BIST logic controller is separate from said embedded memory arrays and operates at a lower frequency than said embedded memory arrays ~~using a remote BIST logic controller that operates at a first frequency, wherein said remote BIST logic controller is separate from said embedded blocks of test logic~~;

sending, by said BIST logic controller, ~~BIST~~ instructions ~~from said remote BIST logic controller said embedded~~ a plurality of blocks of test logic,

wherein said sending comprises using a bus connecting said BIST logic controller to said blocks of test logic so as to allow communication from said BIST logic controller to said blocks,

wherein said bus operates at said lower frequency of said BIST logic controller,

wherein each one of said blocks is incorporated into a corresponding one of said embedded memory arrays and operates at a same frequency as said corresponding one of said embedded memory arrays,

wherein said same frequency comprises a higher frequency relative to said lower frequency of said BIST logic controller and said bus ~~at said first frequency~~; and

performing, by each of said blocks, test functions unique to said corresponding one of said embedded memory arrays, wherein said performing comprises:

increasing the frequency of ~~BIST~~ said instructions to said higher frequency ~~received from said BIST logic controller, using said embedded blocks of test logic, to a second frequency higher than said first frequency~~.

30. (Cancelled).

31. (Currently Amended) The method in claim [[29]] 32, ~~further comprising performing unique testing via logic blocks that are unique to a corresponding embedded memory array at each of said embedded blocks of test logic~~ wherein said performing of data address control generation and said performing of said redundancy allocation are based on said individual micro-instructions.

32. (Currently Amended) The method in claim 29, wherein said performing, by each of said blocks, comprises: ~~each of said embedded blocks of test logic performs the following processes~~:

~~multiplying BIST instructions received from said remote BIST logic controller;~~

performing redundancy allocation;

performing data address control ~~and~~ generation; and

decoding each of said instructions ~~macro instruction sets~~ received from said ~~remote~~ BIST logic controller into individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

33. (Currently Amended) The method in claim 29, The method in claim 22, wherein said performing by said BIST logic controller of said test functions common to all of said embedded memory arrays and said performing by said each of said blocks of said test

functions unique to said corresponding one of said embedded memory arrays ~~said sending process performed by said remote BIST logic controller~~ enables in parallel testing of at least one of the following:

different types of embedded memories, wherein said different types comprise at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

34. (Currently Amended) The method in claim 29, further comprising storing said instructions ~~macro instruction sets~~ in one of read only memories (ROMs), a scannable read only memory (SROM), and other type of memory in said ~~remote~~ BIST logic controller.

35. (Currently Amended) The method in claim 29, wherein said performing by said BIST logic controller of said test functions common to all of said embedded memory arrays comprises performing: ~~further comprising providing, by said remote BIST logic controller~~:

branch prediction;

program counter management;

utility counting; and

general BIST operation control and diagnostic outputs.